WHAT IS CLAIMED IS:

1. An information processing apparatus comprising:

a first oscillating circuit for generating a first clock signal, the first oscillating circuit being capable of operating on a power supply voltage equal to or higher than a first lowest operating voltage;

a second oscillating circuit for generating a second clock signal, the second oscillating circuit being capable of operating on the power supply voltage equal to or higher than a second lowest operating voltage that is higher than the first lowest operating voltage;

a switching circuit that, based on the power supply voltage, selects either the first clock signal or the second clock signal to output as a clock signal; and

an information processing unit, in synchronism with the clock signal, for performing information processing.

2. An information processing apparatus according to claim 1,

wherein the switching circuit outputs the first clock signal as the clock signal when the power supply voltage is equal to or higher than the first lowest operating voltage and lower than the second lowest operating voltage and outputs the second clock signal as the clock signal when the power supply voltage is equal to or higher than the second lowest operating voltage.

3. An information processing apparatus according to claim 1 or 2, further comprising a power supply voltage measuring circuit for measuring voltage of the power supply.

4. An information processing apparatus comprising:

a first oscillating circuit that generates a first clock signal by oscillation and has a first oscillation stability time, the first oscillation stability time being a time required for frequency of the first clock signal becoming stable from beginning of the oscillation;

a second oscillating circuit that generates a second clock signal by oscillation and has a second oscillation stability time, the second oscillation stability time being a time required for frequency of the second clock signal becoming stable from beginning of the oscillation, and being longer than the first oscillation stability time;

a switching circuit for, based on an elapsed time of the first oscillating circuit from the beginning of the oscillation and an elapsed time of the second oscillating circuit from the beginning of the oscillation, selecting and outputting either the first clock signal or the second clock signal as the clock signal; and

an information processing unit for, in synchronism with the clock signal, performing information processing.

5. An information processing apparatus according to claim 4,

wherein the switching circuit selects the first clock signal after the first oscillation stability time has passed until the second oscillation stability time comes, and selects the second clock signal after the second oscillation stability time has passed.

6. An information processing apparatus according to claim1, 2, 4, or 5,

wherein the first oscillating circuit is a CR oscillating circuit, a quartz oscillating circuit, or a ceramic oscillating circuit, and

the second oscillating circuit is a PLL oscillating circuit.

7. An information processing apparatus according to claim 3,

wherein the first oscillating circuit is a CR oscillating circuit, a quartz oscillating circuit, or a ceramic oscillating circuit, and

the second oscillating circuit is a PLL oscillating circuit.

8. An information processing apparatus according to claim 4,

wherein the first oscillating circuit is a CR oscillating circuit, a quartz oscillating circuit, or a ceramic oscillating circuit,

the second oscillating circuit is a PLL oscillating circuit, and

the switching circuit outputs the first clock signal as the clock signal until the PLL oscillating circuit establishes synchronization, and outputs the second clock signal as the clock signal after the PLL oscillating circuit establishes synchronization and a state of the PLL oscillating circuit reaches a synchronization maintained state.

9. An information processing apparatus according to claim 8,

wherein the switching circuit, when the PLL oscillating circuit outputs a lockup signal, detects completion of the synchronization.

10. An information processing apparatus according to claim 7, wherein the PLL oscillating circuit comprises:

a voltage controlled oscillator for outputting an oscillation signal having a frequency which corresponds to a voltage control signal;

a phase comparator that compares phase of a reference clock signal and phase of a comparison oscillation signal and outputs a comparison signal;

a low pass filter for passing a lower component of the comparison signal;

a divider for dividing the oscillation signal and outputting the comparison oscillation signal;

an offset voltage generating unit for generating an offset voltage; and

an adder for adding an output signal of the low pass filter and the offset voltage to output the voltage control signal.

11. An information processing apparatus according to claim 10,

wherein the offset voltage generating unit comprises:

an offset voltage data storage unit for storing an offset voltage data in advance; and

a D/A converter for converting the offset voltage data to the offset voltage.

12. An information processing apparatus according to claim 11,

wherein the PLL oscillating circuit further comprises an offset voltage data generating unit for, based on the voltage control signal at a prescribed lockup state of the PLL oscillating circuit, generating the offset voltage data.

13. An information processing apparatus according to claim 10, wherein the offset voltage generating unit comprises:

a voltage dividing unit for dividing prescribed power supply voltage to generate a plurality of divided voltage; and

a voltage selection unit for selecting one divided voltage from the plurality of the divided voltage as the offset voltage.

14. An information processing apparatus according to claim 10,

wherein the offset voltage generating unit comprises a voltage dividing unit for dividing prescribed voltage to generate the offset voltage.

15. An information processing apparatus according to claim 12,

wherein the prescribed lockup state is a state where the PLL oscillating circuit is, when the offset voltage generating unit does not output the offset voltage, locked up so that the oscillation signal has a prescribed frequency.

16. An information processing apparatus according to claim 12, wherein the PLL oscillating circuit comprises:

a controlled voltage determining unit for determining voltage of the voltage control signal at a prescribed timing;

an offset data correction unit for, based on a result of determination of the controlled voltage determining unit, correcting the offset voltage to make a new offset voltage.

17. In a control method for an information processing apparatus, the information processing apparatus comprising:

an information processing unit for, based on a clock signal, carrying out various information processing operations;

a first oscillating circuit that generates a first clock signal and is able to operate on power supply voltage equal to or higher than a first lowest operating voltage,

a second oscillating circuit that generates a second clock signal and is able to operate on the power supply voltage equal to or higher

than a second lowest operating voltage that is higher than the first lowest operating voltage;

a switching circuit for, based on the power supply voltage, outputting either the first clock signal or the second clock signal as the clock signal;

the control method comprising:

determining power supply voltage;

outputting by the switching circuit the first clock signal as the clock signal when the power supply voltage is equal to or higher than the first lowest operating voltage and lower than the second lowest operating voltage; and

outputting by the switching circuit the second clock signal as the clock signal when the power supply voltage is equal to or higher than the second lowest operating voltage.

18. In a control method for an information processing apparatus, the information processing apparatus comprising:

a first oscillating circuit that generates a first clock signal by oscillation and has a first oscillation stability time, the first oscillation stability time being a time required for frequency of the first clock signal becoming stable from beginning of the oscillation;

a second oscillating circuit that generates a second clock signal by oscillation and has a second oscillation stability time, the second oscillation stability time being a time required for frequency of the second clock signal becoming stable from beginning of the oscillation, and being longer than the first oscillation stability time;

a switching circuit for, based on an elapsed time from the beginning of the oscillation of the first oscillating circuit and on an elapsed time from the beginning of the oscillation of the second oscillating circuit, selecting to output either the first clock signal or the second clock signal as a clock signal;

an information processing unit for, in synchronous with the clock signal, carrying out information processing operations;

the control method comprising:

outputting the first clock signal as the clock signal after the first oscillation stability time has passed until the second oscillation stability time comes, and the second clock signal as the clock signal after the second oscillation stability time has passed.

19. A method for an information processing apparatus according to claims 17 or 18

wherein the second oscillating circuit is a PLL oscillating circuit with a voltage controlled oscillator that outputs an oscillation signal having frequency corresponding to voltage of a voltage control signal; and

the method further comprising:

applying a prescribed offset voltage to the voltage controlled

oscillator as the voltage control signal.

20. A method for an information processing apparatus according to claims 19,

wherein the prescribed offset voltage is a voltage of the voltage control signal, when the PLL oscillating circuit is locked up so that the oscillation signal has a prescribed frequency.

21. A method for an information processing apparatus according to claims 19 or 20, further comprising:

determining voltage of the voltage control signal at a prescribed timing; and

correcting the offset voltage to make a new offset voltage based on determined voltage of the voltage control signal.

22. A control program executed by an information processing apparatus, the information processing apparatus comprising:

an information processing unit for, based on a clock signal, carrying out various information processing operations;

a first oscillating circuit that generates a first clock signal and is able to operate on power supply voltage equal to or higher than a first lowest operating voltage,

a second oscillating circuit that generates a second clock signal and is able to operate on the power supply voltage equal to or higher than a second lowest operating voltage that is higher than the first lowest operating voltage; and

a switching circuit for, based on the power supply voltage, outputting either the first clock signal or the second clock signal as the clock signal;

the control program comprising the routines of:

determining the power supply voltage;

outputting to the switching circuit the first clock signal as the clock signal when the power supply voltage is equal to or higher than the first lowest operating voltage and is lower than the second lowest operating voltage; and

outputting to the switching circuit the second clock signal as the clock signal when the power supply voltage is equal to or higher than the second lowest operating voltage.

23. A control program executed by an information processing apparatus, the information processing apparatus comprising:

an information processing unit for, in synchronous with a clock signal, carrying out various information processing operations;

a first oscillating circuit that generates a first clock signal by oscillation and has a first oscillation stability time, the first oscillation stability time being a time required for frequency of the first clock signal becoming stable from beginning of the oscillation;

a second oscillating circuit that generates a second clock signal by oscillation and has a second oscillation stability time, the second oscillation stability time being a time required for frequency of the second clock signal becoming stable from beginning of the oscillation, and being longer than the first oscillation stability time;

a switching circuit for, based on an elapsed time from the beginning of the oscillation of the first oscillating circuit and on an elapsed time from the beginning of the oscillation of the second oscillating circuit, selecting to output either the first clock signal or the second clock signal as a clock signal;

the control program comprising the routines of:

outputting the first clock signal as the clock signal after the first oscillation stability time has passed until the second oscillation stability time comes, and the second clock signal as the clock signal after the second oscillation stability time has passed.

24. A control program executed by an information processing apparatus according to claims 22 or 23,

wherein the second oscillating circuit is a PLL oscillating circuit with a voltage controlled oscillator that outputs a oscillation signal having frequency corresponding to voltage of a voltage control signal; and

the control program further comprises the routines of applying a prescribed offset voltage to voltage of the voltage control signal.

25. A control program executed by an information processing apparatus according to claim 24,

wherein the prescribed offset voltage is set to voltage of the voltage control signal, the voltage being a voltage attained,when the offset voltage is not applied to the PLL oscillating circuit, when the PLL oscillating circuit is locked up so that the oscillation signal has a prescribed frequency.

26. A control program executed by an information processing apparatus according to claim 24, further comprising the routines of;

determining voltage of the voltage control signal at a prescribed timing; and

correcting the offset voltage to make a new offset voltage based on the determined voltage of the voltage control signal.